AN 8-18 GHz MONOLITHIC TWO-STAGE LOW NOISE AMPLIFIER*

L. C. T. Liu, D. W. Maki, C. Storment, M. Sokolich and W. Klatskin

Torrance Research Center
Hughes Aircraft Company
3100 W. Lomita Boulevard
P.O. Box 2999
Torrance, CA 90509

ABSTRACT

A wideband monolithic low noise amplifier which covers the frequency band from 8 to 18 GHz has been designed and fabricated. The amplifier has a noise figure less than 4.3 dB and an associated gain of 8.5 dB across the entire band. A revised version of the amplifier which has a design goal of sub-four dB noise figure and an associated gain of 12 dB has been processed. Measured data will be presented at the conference.

INTRODUCTION

GaAs monolithic microwave integrated circuits (MMICs) have become practical components for various system applications due to recent advances in material processing technology. The monolithic low noise amplifier is an essential functional chip for a number of applications as it determines the overall system noise figure. Recent papers have demonstrated the potential of the monolithic low noise amplifier and shown good results at X-band.[1-2]

There is growing interest within the government for multifunction radar systems which cover much wider bandwidths than the conventional 10 percent. A typical application is multiband radar covering both X- and Ku-band. Monolithic ICs offer significant advantages in wideband circuits since the matching can be done very closely to the device.

In this paper, details of an 8-18 GHz two-stage monolithic low noise amplifier will be presented. The circuit design and fabrication process will be discussed and the RF performance will be shown. Finally, an analysis of the measured results and a revised design of the amplifier will be discussed.

CIRCUIT DESIGN

The broadband monolithic low noise amplifier design is based on Hughes low noise GaAs MESFETs operating over X- and Ku-band.[3] These FETs have a gate dimension of 0.5 by 300 μm, and a minimum noise figure of 1.7 dB with an average associated gain of 9.5 dB at 12 GHz. An equivalent circuit of the device is derived from the measured S-parameters. Based on this equivalent circuit and the noise model given by Podell, Ku and Liu,[4] the minimum noise figure and optimum source admittance are obtained at the frequency band of interest.

An input matching network is synthesized[5] to provide the optimum source admittance for noise figure to the input port of the device over the full band. An interstage matching network is then synthesized to obtain the gain match between the output port of the first device to the input port of the second device. Finally, an output matching network is used to match to the 50 ohm load.

Figure 1 illustrates the schematic of this low noise amplifier. The characteristic impedances of all the transmission lines are between 47 and 56 ohms to facilitate the realization of the amplifier. The line lengths are references at 1 GHz, and are all appropriate for monolithic layout. In the amplifier design, a very simple configuration has been chosen to assure that high yield can be achieved in the wafer processing. The calculated performance of this amplifier is illustrated in Figure 2. The noise figure is below 4 dB across the entire frequency band with an average associated gain of 12 dB.

A completed amplifier chip is shown in Figure 3. As can be seen from the figure, the amplifier uses two 0.5x300 μm FETs as active devices. MOM capacitors are employed for both RF bypass and DC blocking applications. High airbridges fabricated on 6 μm thick photoresists are used to connect the source pads and to interconnect the microstrip lines to the top plates of the MOM capacitors. Microstrip transmission lines are used due to their low loss, low dispersion and useful impedance range. The amplifier was designed to use via hole grounding but was laid out to use over the edge (OTE) grounds if desired. The chip size is 1.52 x 2.0 x 0.1 mm.

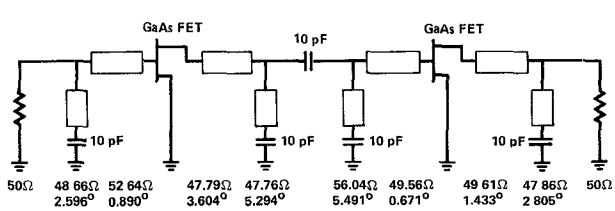

Fig. 1 Schematic of 8-18 GHz amplifier.

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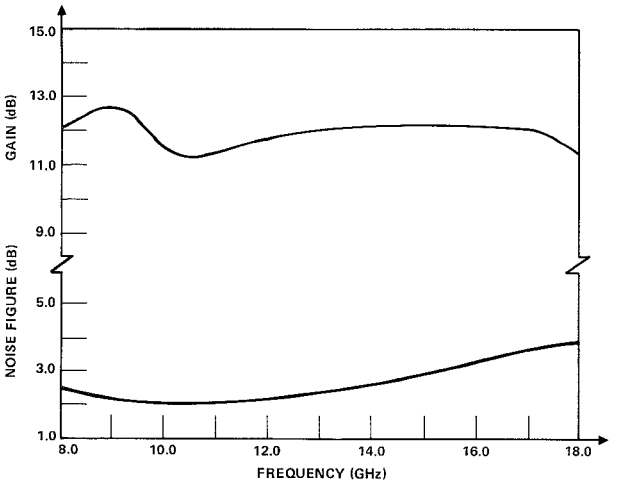

Fig. 2 Calculated performance of 8-18 GHz amplifier.

WAFER FABRICATION

Horizontal Bridgeman grown Cr-doped semi-insulating substrates are used for the amplifier fabrication. Also used are Cr-doped substrates with a 2 μm-thick unintentionally doped VPE buffer layer. The latter material is used to improve the uniformity of the active layer. The active channel layer is formed using silicon ion implantation with a dose of $6 \times 10^{12} cm^{-2}$ at 100 KeV. Isolation between FETs is achieved by either proton bombardment or mesa etch. Source-drain ohmic contacts are deposited and alloyed. Slightly recessed gates are defined either using a conventional photolithography or E-beam direct write system to give a gate length of 0.5 to 0.7 μm.

The source-drain overlay metal is deposited to a thickness of 1.5 μm to form the RF circuitry and the bottom plates of the MOM capacitors. A silicon dioxide layer with a thickness of 2000 Å is sputtered for the overlay capacitor. Cr-Au top metal layers and airbridges for interconnection are then formed. The wafers are thinned to 0.1 mm and via holes are etched from the back of the wafer. Finally, via holes and the back of the wafer are metallized. Amplifier chips can be obtained by sawing the wafers.

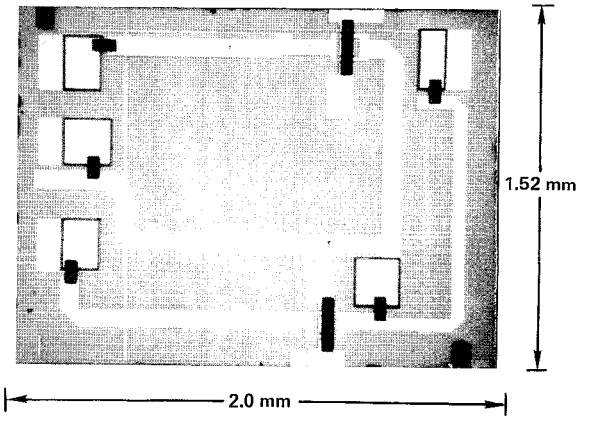

Fig. 3 8-18 GHz monolithic low noise amplifier.

RF PERFORMANCE

A number of wafers have been processed for this 8-18 GHz monolithic low noise amplifier and amplifier chips have been extensively tested. In the characterization, each FET on the amplifier chip can be biased individually. When both FETs are biased for low noise operation, i.e., $V_{D1} = V_{D2} = 3V$, $I_{D1} = I_{D2} = 12$ mA, the amplifier has an average gain of 8.5 dB over the frequency band from 8 to 18 GHz. The noise figures of the amplifier are 4.3 and 4.2 dB at 18 and 12 GHz respectively. The associated gain is lower than the 12 dB predicted by computer simulation. The measured noise figure and gain response are shown in Figure 4.

As described before, both via hole and over the edge grounds can be used for this amplifier. One wafer of amplifiers, LNA 266, was split into two pieces, one receiving via hole, the other using wire bond grounds. The gain of the via holed device was consistently 1 to 2 dB greater than that of the circuits using wire bonds.

AMPLIFIER DIAGNOSIS

FETs from the amplifier chips were scribed free and tested as discrete devices from 2 to 18 GHz using an automatic network analyzer. Comparison of the measured S-parameters of the FET from wafer LNA 290 to those of a discrete FET which was used in the amplifier design shows that the magnitude of S_{21} of the FET from the amplifier chip is lower than that of the discrete FET. In turn, this causes the gain in the amplifier to drop. Also, this excised FET has a larger output reflection coefficient (S_{22}) than that of the discrete FET. Figure 5 shows the measured S-parameters of both FETs. We believe that the variation in the FET is caused first by the redistribution of the Cr in the Cr-doped GaAs substrate, which changes the doping profile of the active layer and secondly, by the possible damage to the active channel during the proton bombardment process because a photoresist layer was too thin to protect the active region. The

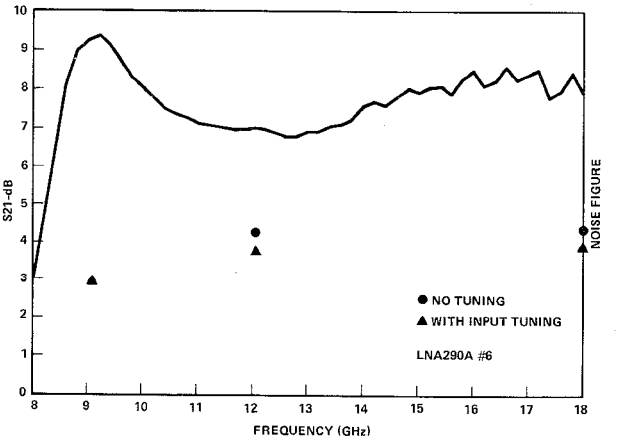

Fig. 4 Gain and noise figure of the 8-18 GHz LNA.

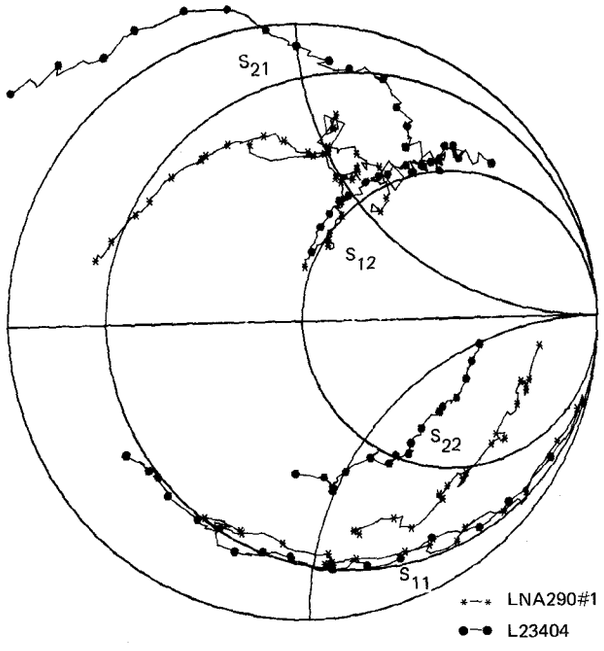

Fig. 5 S-parameters of the 0.5 μm GaAs FET.

first problem (Cr redistribution) can be solved by fabrication active layers using ion implantation into a VPE buffer. Tighter control of the photoresist thickness will eliminate the second problem (channel damage).

A second version of the amplifier has been designed and is being fabricated. In the new design, via holes are the only means of obtaining grounding. This eliminates the need to bring all ground pads to the edge of the chip, and it makes layout of the circuitry more flexible. Two via holes are employed for each FET to reduce the source inductance. Figure 6 shows a photograph of an amplifier chip from this wafer. Data from the amplifiers will be presented at the conference.

CONCLUSIONS

An 8 to 18 GHz monolith low noise amplifier has been developed successfully. The RF performance of this amplifier satisfies a broad range of applications and can be used as an inexpensive gain block.

ACKNOWLEDGMENTS

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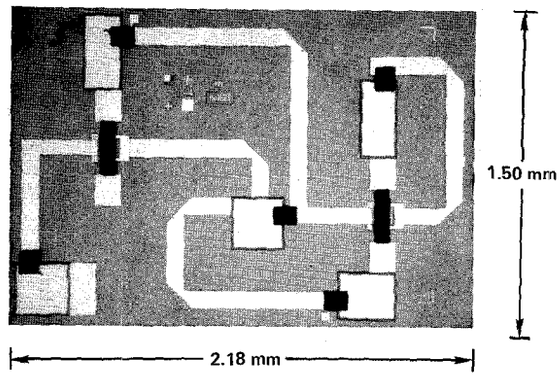

Fig. 6 Revised version of 8-18 GHz monolithic low noise amplifier.

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